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Investor Presentation

June 2022

Safe Harbor

This presentation contains forward-looking statements concerning Atomera Incorporated (""Atomera," the "Company," "we," "us," and "our"). The words "believe," "may," "will," "potentially," "estimate," "continue," "anticipate," "intend," "could," "would," "project," "plan," "expect" and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section "Risk Factors" included in our Annual Report on Form 10-K filed with the SEC on February 15, 2022. In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

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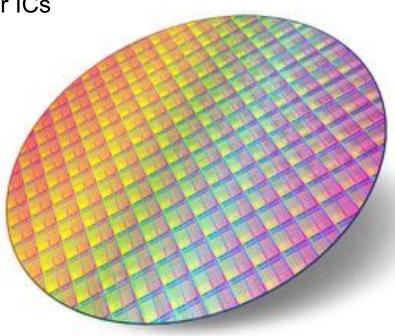
Investment Overview

Mears Silicon Technology (MST[®]) is a thin film used to enhance semiconductors

Results in higher performance, lower power, and lower costs for ICs

Capital-light IP and technology licensing business

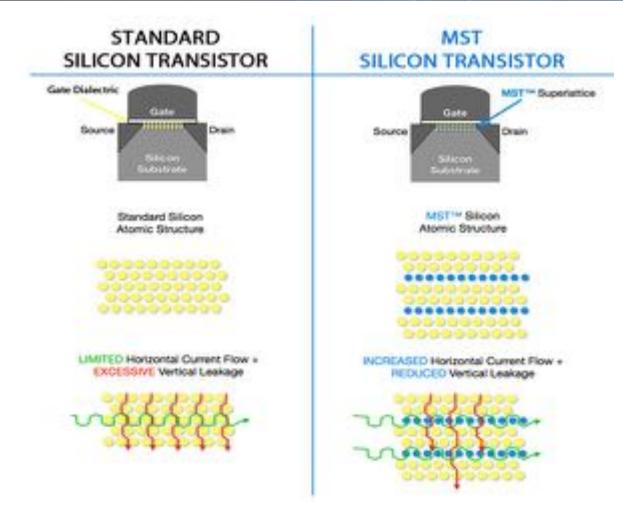
- Robust and growing patent portfolio
- Engaged with 50% of world's top semiconductor makers
- Licenses with five companies including two JDAs
 - Successfully completed 1st JDA's technical objectives
- Strong team to commercialize technology



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MST Technology

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Potential Benefits

Improved Efficiency

- Higher transistor performance
- Lower power consumption
- Better reliability

Lower cost

- Reduced die size
- Improved yield

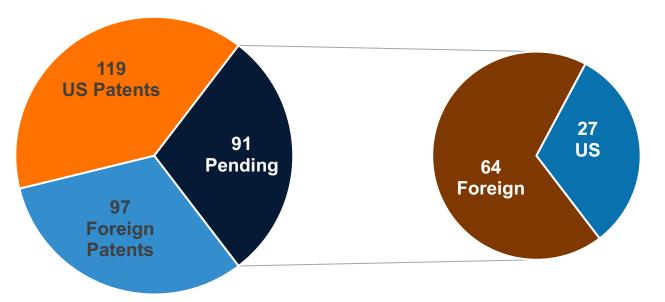
AND THE CONTRACTOR

Higher throughput

Same benefits as a node shrink

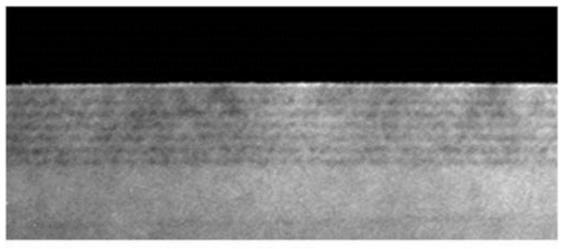
Strong and Defensible IP Portfolio

307 Patents Issued and Pending



Discoverable These distinctive layers are visible on products using MST

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Core MST Method and Device MST Enabled Devices/Architecture Next-Gen Architectures using MST

Extensive know-how Extends life and value of patents

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Target Customers & Partners





Tool Suppliers (Partners)

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Customer Engagement & Revenue Model

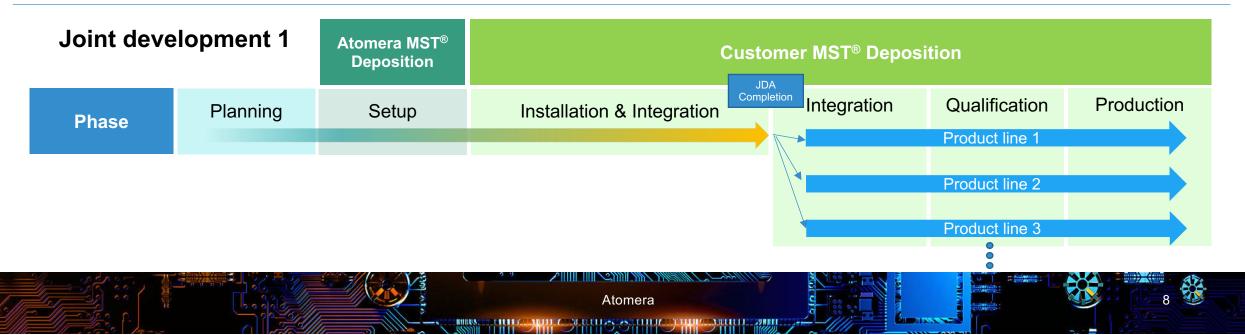
		Customer Wafer Manufacturing									
		Atom	era MST [®] Deposition	Cust	Customer MST [®] Deposition						
Phase	1. Planning	2 . Setup	3. Integration	4. Installation	5. Qualification	6. Production					
		Engineering S Fees	 MST deposition of Integration const 	on customer wafe ulting	rs						
			License Fees	 Integration lice Manufacturing Distribution lice 	<mark>j licenses</mark>						
			Joint Development A	Agreements		Royalties					
			Atomera Incorporated								

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Customer Engagement Model

Standard	customer		Customer Wafer Manufacturing								
engageme	ent	Atom	nera MST [®] Deposition	Customer MST [®] Deposition							
Phase	Planning	Setup	Integration	Installation	Qualification	Production					

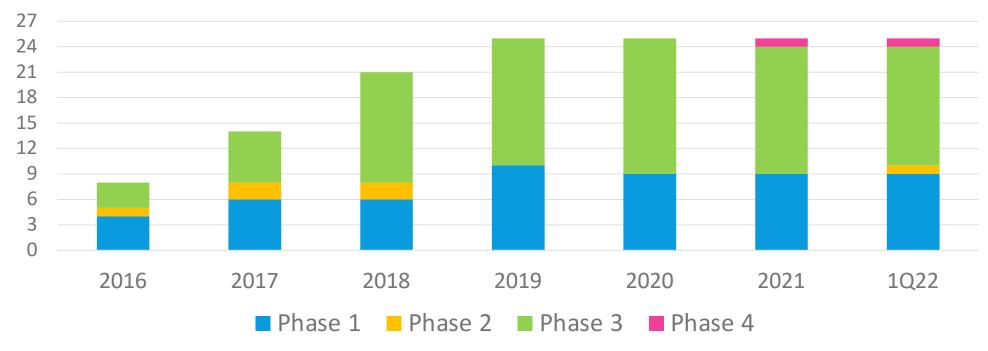
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Customer Pipeline

Number of Customer Engagements

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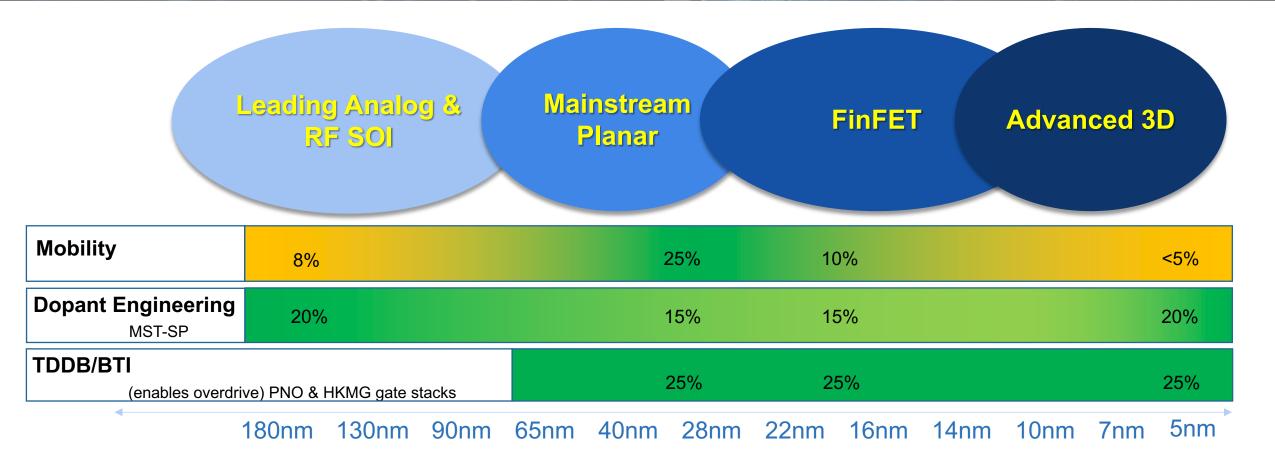


- 19 customers, 25 engagements
- Working with 50% of the world's top semiconductor makers*

• 10 of the top 20 (IC Insights, McClean Report 2021)

^ End of year engagement count, plus CY quarters

MST Key Benefits Across Nodes



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These Benefits are ADDITIVE & COMPLEMENTARY to other enhancement technologies



MST technology focus areas

• atomera MST for Advanced Nodes

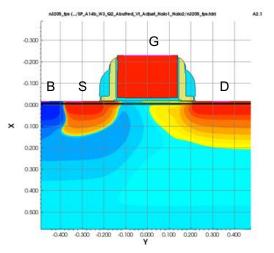
MST-SP

MST for RF-SOI

MST-SP

MST-SP is a highly-engineered asymmetric power device

- Uses MST to enhance Idlin and precisely control dopant profiles
- Improves 5V power devices
 - Lower R_{SP}
 - Can be traded for up to 20% smaller area
- Targeted for rapidly-growing PMIC market



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5V Transistors – Critical and Growing Market

• Targeted at rapidly-growing PMIC (Power Management IC) market

- Power devices can be up to 80% of PMIC die area
- All ICs need stable, regulated power
 - Across battery charge level, lifetime degradation, and load
 - Across usage modes DVS (Dynamic Voltage Scaling), sleep, others
- 5V transistor required to deliver IC power from any source
 - Battery-powered, USB, wall connected
- 5V devices do not scale with Moore's Law
- MST SP allows significant scaling of gate length, and a performance boost

2018-2025F IC Market Forecast by Device Type (Analog)

Product Category	18	19	19/18 % Chng	20	20/19 % Chng	21F	21/20 % Chng	22F	22/21 % Chng	23F	23/22 % Chng	24F	24/23 % Chng	25F	25/24 % Chng	20-2 CAG
Power Management (SM)	14,529 69,243 \$0.21	14,050	-3%	14,640	4%	18,153	24%	20,332	12%	22,568	11%	23,019	2%	24,861	8%	119
Units (M)	69,243	67,227	-3%	68,409	2%	80,788	18%	91,396	13%	102,475	12%	105,580	3%	115,178	9%	119
ASP (\$)	\$0.21	\$0.21	0%	\$0.21	2%	\$0.22	5%	\$0.22	-1%	\$0.22	-1%	\$0.22	-1%	\$0.22	-1%	0%

THE WALL STREET JOURNAL.

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"A typical 5G smartphone can hold as many as eight powermanagement chips, compared with two to three in a 4G phone, according to Hui He, an analyst at research firm Omdia."

WSJ "Why the Chip Shortage is So Hard to Overcome" 4/20/2021

Source: IC Insight's McClean Report, June 2021

Example: Use Of 5V Transistor In Apple iPhone13



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- 5V transistor assessment by Atomera

Reference https://www.techinsights.com/blog/teardown/apple-iphone-13-pro-teardown?utm source=Prospect+Email&utm medium=Email&utm campaign=2021+-+Q3+-+Teardown+-+Blog-+Apple+iPhone+13

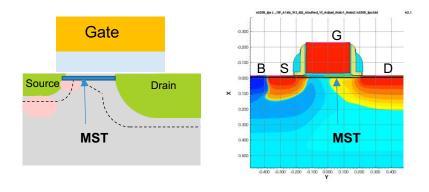
5V MST-SP Product – Value Proposition

Industry best performance at 180nm (Rsp)

- Based on measured silicon data
- Scalable to smaller process nodes
- Meets all reliability requirements
 - Breakdown Voltage (BVDSS) > 10.5V

Significant cost savings, performance benefits

- Die area reduction up to 20%
- Demonstrates the big advantage MST can bring to highly optimized designs
- Complete design package accelerates time to production



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Royalty Opportunity

- ~410 wafer fabs operating worldwide
- Adoption of MST in one fab can make Atomera profitable from royalties alone
 - 2022 non-GAAP OPEX guidance is \$15.25M \$15.75M

Example 1 Worldwide Avera	ge Fab	Example 2 Leading Foundry, 28nm Fab					
Monthly Fab Capacity ¹ (wafers/month)	46,240	Monthly Fab Capacity (wafers/month)	80,000				
Industry average wafer ASP - 2018	\$1,365	Industry average 28nm wafer ASP	\$3,300				
Annual Revenue Potential ²	\$15.1M	Annual Revenue Potential ²	\$63M				
Annual Revenue at 50% of ramp ²	\$7.6M	Annual Revenue at 50% of ramp ²	\$31.7M				

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1. Represents wafers starts per month (200mm equiv) – 227.5M starts in 410 fabs

2. Assumes 2% royalty rate

Source: IC Insights Global Wafer Capacity 2021-2025 report, McClean Report 2021, 2022

MST Customer Business Opportunity

Foundry economics

	/afer rice	GM%	M\$ rease	/IST yalty	-	Vafer Cost	
28nm HP wafer	\$ 3,300	45%	\$ -	\$ -	\$	1,815	
28nm HP+ wafer	\$ 3,450	45%	\$ 68	\$ -			5% higher price for +15% performance boost
28nm HP wafer with MST	\$ 3,600	47.0%	\$ 208	\$ 72	\$	1,907	30% performance boost=10% higher price (+ \$20 MST cost)
28nm HP wafer with MST	\$ 3,713	48.6%	\$ 318	\$ 74	\$	1,909	25% die shrink=12.5% price increase (+ \$20 MST cost)

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• Gross margin increases by \$200-\$300 per wafer after foundry pays Atomera royalties

Fabless semiconductor economics

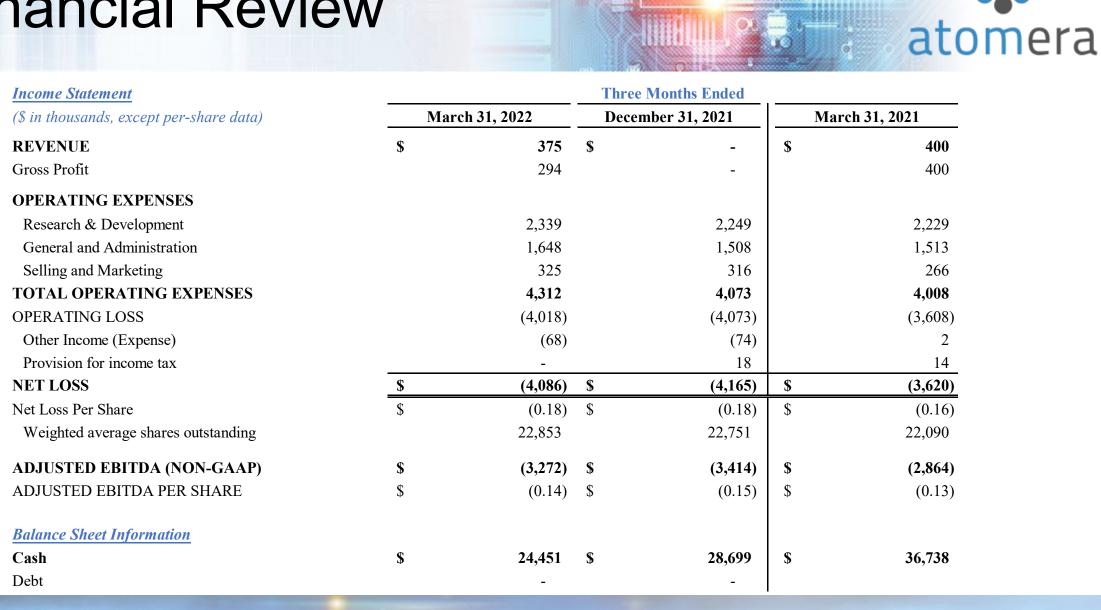
	Chip sales/ wafer	GM%	GM\$ Increase	Product ASP	Die/wafer	
28nm HP wafer	\$ 9,233	50%	\$-	\$ 4.86	2,235	Baseline business for 30mm ² chip
28nm HP wafer with MST	\$ 12,398	59%	\$ 3,165	\$ 4.86	3,001	Improved financials with 25% size reduction

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Sales and profit both increase by over \$3000 per wafer for fabless manufacturer

Everyone in the value chain benefits from MST technology

Financial Review



Summary

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High margin, recurring revenue financial model

- Strong technology, patent position, and balance sheet
- Traction with many top industry players and growing licensee base
- Ramping commercial license revenues

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Thank You